SUBCONTRACT TITLE**:** **FABRICATION AND PHYSICS OF CDTE DEVICES BY SPUTTERING**

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QUARTERLY TECHNICAL STATUS REPORT FOR**: Phase 1/Quarter 1**

SUBMITTED TO**:** **Ken Zweibel**
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This progress report covers the first quarter of Phase 1 for the period March 1, 2005, through May 30, 2005, of the above Thin Film Photovoltaic Partnership Program subcontract.

During this quarter we worked on ellipsometric diagnostics, device physics modeling and thin CdTe solar cell limitations. In this report we highlight our recent results on real-time spectroscopic ellipsometry studies of rf-sputtered solar cells (task 1.3.2) and quantitative estimates of nonuniformity loss in solar cell modules, including the effect of series resistance (task 1.2.3).

Task 1.3.2 Real Time Spectroscopic Ellipsometry (SE)

In SE studies of the microstructure of deposited solar cells (without back contacts), Br_2/methanol etches have been used with the initial intent being to remove oxide layers so that the deduced SE pseudo-dielectric function is more closely representative of the true dielectric function. In addition to removing oxide, a series of successive etching steps also step-wise smoothens the surface simultaneously with reducing the bulk layer thickness. Once the surface roughness thickness has stabilized, thickness reduction of the bulk layer occurs essentially layer-by-layer with a thickness loss per etch step that depends on the Br_2 concentration in methanol. Thus, by performing numerous etching/measurement cycles, we simulate a real time spectroscopic ellipsometry measurement, but in time reverse. For example, Figure 1(a) shows the CdTe surface roughness thickness and bulk layer void fraction during etching of a $CdCl_2$-treated solar cell fabricated at Univ. Toledo. Each point represents an etching step that leads to a reduction in the bulk layer thickness of the CdTe, starting from an initial thickness of 2.1 μm. The thickness of the CdTe is determined from an analysis of data at low energies (≤ 1.45 eV) where thin film interference oscillations are present. The surface

roughness thickness and bulk layer void volume fraction are determined from the data at high energies (≥ 3 eV) where the CdTe is opaque and high surface sensitivity is attained. The solar cell was deposited on TEC-15 glass; however, the back-contact process steps were omitted for access to the back of the cell. Figure 1 shows that after ~8 etching steps the surface roughness and void fraction stabilize with relatively small variations thereafter. With successive etching steps, the surface roughness shows random fluctuations over the range of ~20-40 Å whereas the void fraction (scaled relative to single crystal CdTe) lies in the range of 0.02-0.03. The void fraction is uniform over a wide range of bulk layer thickness, from 0.64 to 1.7 μm, and is tentatively attributed to a density deficit in the grain boundary regions. Figure 1(b) shows a proposed schematic of the film structure. For a CdTe film of this starting bulk layer thickness (2.1 μm), the roughness is also quite thick (0.3 μm) and is interpreted in the model as a "bulk" layer with a high void fraction (~0.3) which is removed in the etching process.

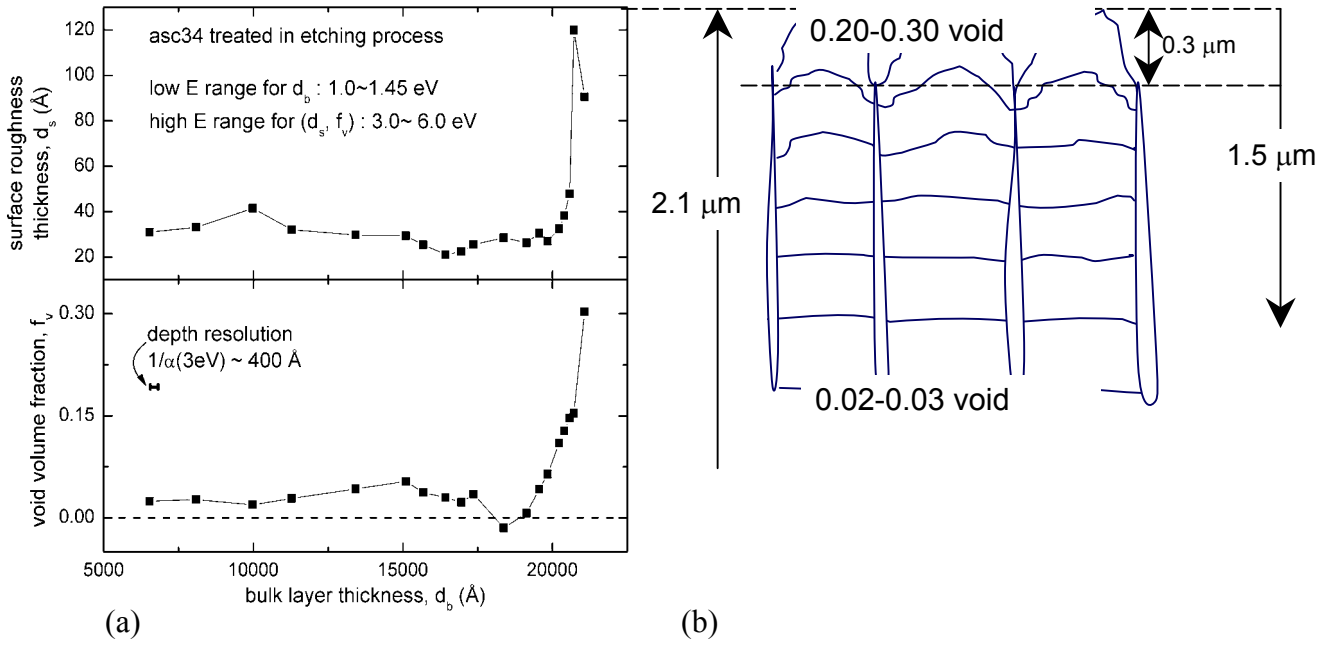

Fig. 1 (a, left) Evolution of the surface roughness thickness and a depth profile of the void volume fraction plotted versus bulk layer thickness obtained in successive Br_2/methanol etching steps that reduce the bulk thickness; (b, right) a schematic structure suggested from (a).

Additional information on the depth profile of the structure can be deduced from the energies and widths of the critical point transitions. The energies remain essentially constant with etching; however, as the CdS interface is approached, reproducible shifts are detected that may be attributed to the presence of S in the CdTe. Unfortunately, it does not appear possible to probe through the CdS/CdTe interface since etching studies of a single CdS film shows that it is disrupted by Br_2/methanol etch, leading to severe roughening and delamination of the CdS. Figure 2(a) shows results for the depth profile of the widths of the prominent E_1 and E_2 critical points. The widths associated with the surface layer are very broad; however, these reach a minimum once the surface layer is removed and the bulk film void fraction stabilizes below 0.03. As etching of the CdTe

progresses toward the CdS interface, the broadening increases. This effect may be attributed to the usual growth mode of physical vapor deposited films in which there is expected to be a gradual increase in average grain size with increasing thickness. The results can be understood using a simple model of independent line broadening mechanisms denoted $h\Delta\nu_i \sim h/\tau_i$ (in photon energy), in which the resultant transition lifetime is given by: $1/\tau = 1/\tau_1 + 1/\tau_2 + \ldots$, e.g., '1': phonon scattering; '2': impurity scattering, etc. For a polycrystalline material, this leads to a resultant linewidth $h\Delta\nu \equiv \Gamma = \Gamma_b + (h\upsilon/R)$; where Γ_b is the single crystal linewidth; $(h\upsilon/R)$ is the grain boundary scattering term, R is the average grain radius, and υ is the electron velocity. Figure 2(b) shows a proposed schematic of the sample structure, a variant on that of Fig. 1(b), that accounts for the decrease in transition widths with increasing thickness shown in Fig. 2(a).

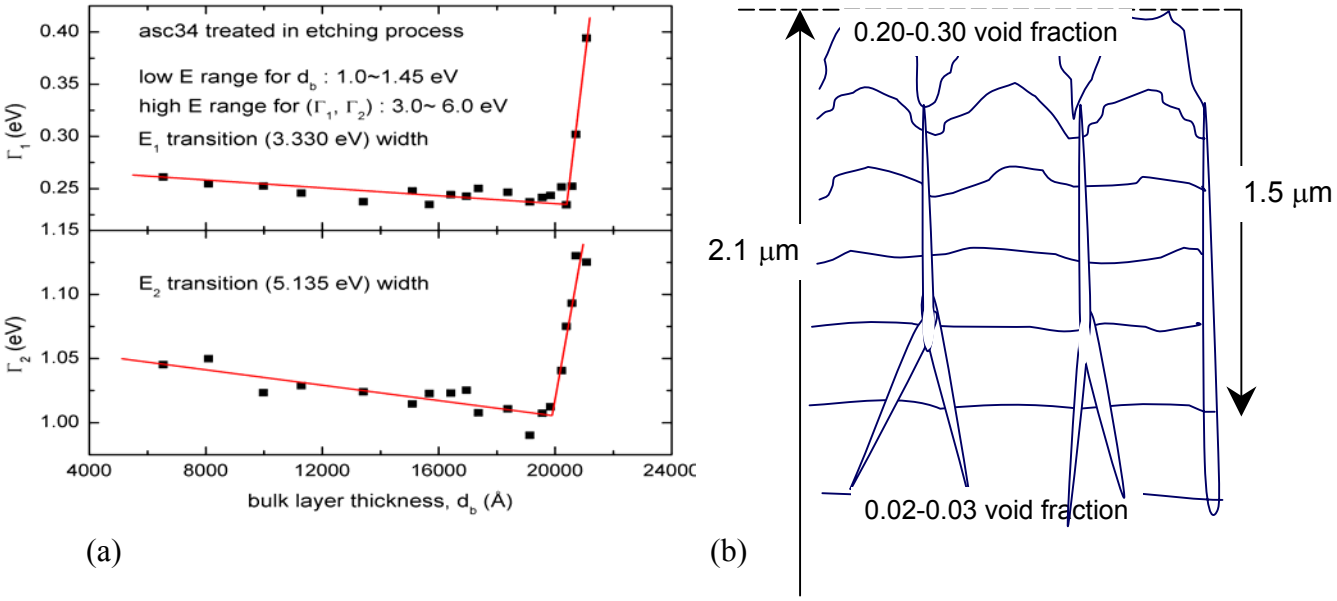

Fig. 2 (a, left) Depth profile of the photon energy widths of the E_1 (3.33 eV) and E_2 (5.14 eV) transitions in CdTe, plotted versus bulk layer thickness obtained in successive Br_2/methanol etching steps that reduce the bulk thickness; (b, right) a schematic structure suggested from (a).

In addition to the structural analyses of Figs. 1 and 2 that focus on the high energy SE data for the CdTe surface roughness and structural depth profiles, it is also possible to extract characteristics of the underlying CdS and its layered structure from the low energy data. This information is obtained from the same low energy data range that provides the CdTe bulk layer thicknesses, plotted along the abscissas in Figs. 1(a) and 2(a). Figure 3 shows deduced SE pseudo-dielectric function spectra (solid lines) obtained after a sufficient number of Br_2-methanol etching steps such that the CdTe surface roughness layer thickness and the CdTe bulk layer void volume fraction have stabilized. Also shown are the results of least-squares regression analysis best fit (broken lines). The multilayer model that leads to this best fit is shown in Fig. 4. The nature of the multiple layers of this model will be described in detail in the next paragraph.

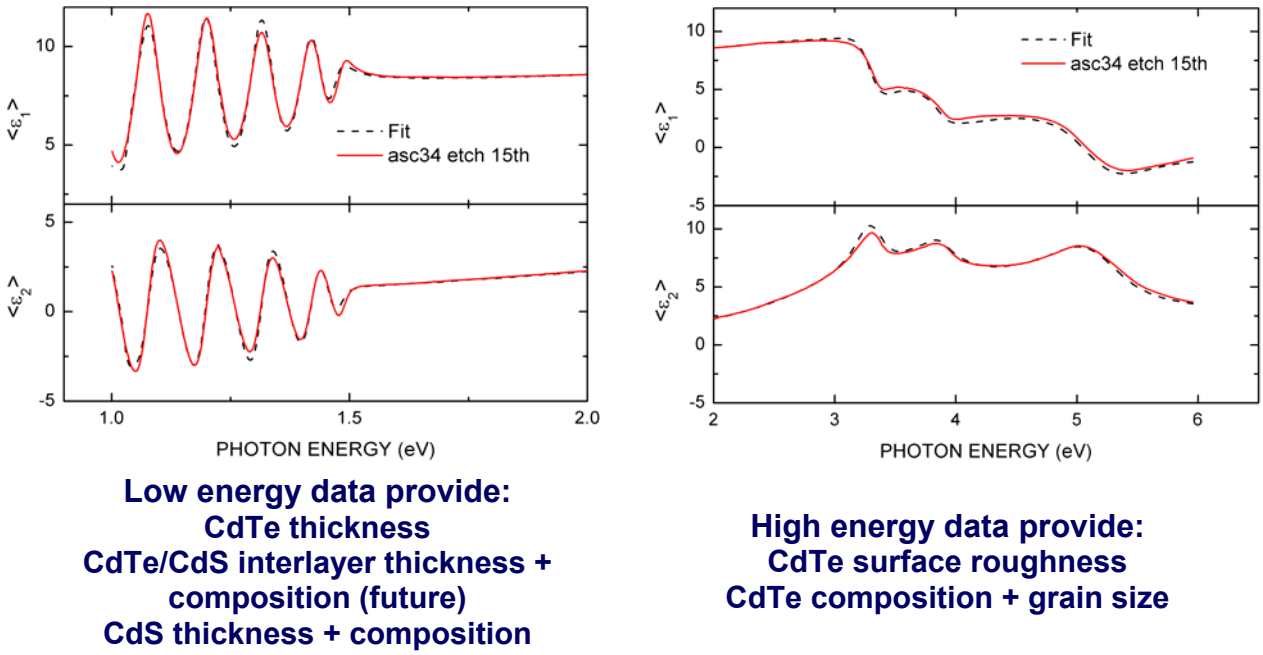

Fig. 3 Experimental pseudo-dielectric function spectra obtained for the same CdTe solar cell as in Figs. 1 and 2 after a sufficient number of etching steps such that the surface roughness layer thickness and the void volume fraction stabilize (solid lines); also shown is the best fit using the structural model of Fig. 4 (broken lines).

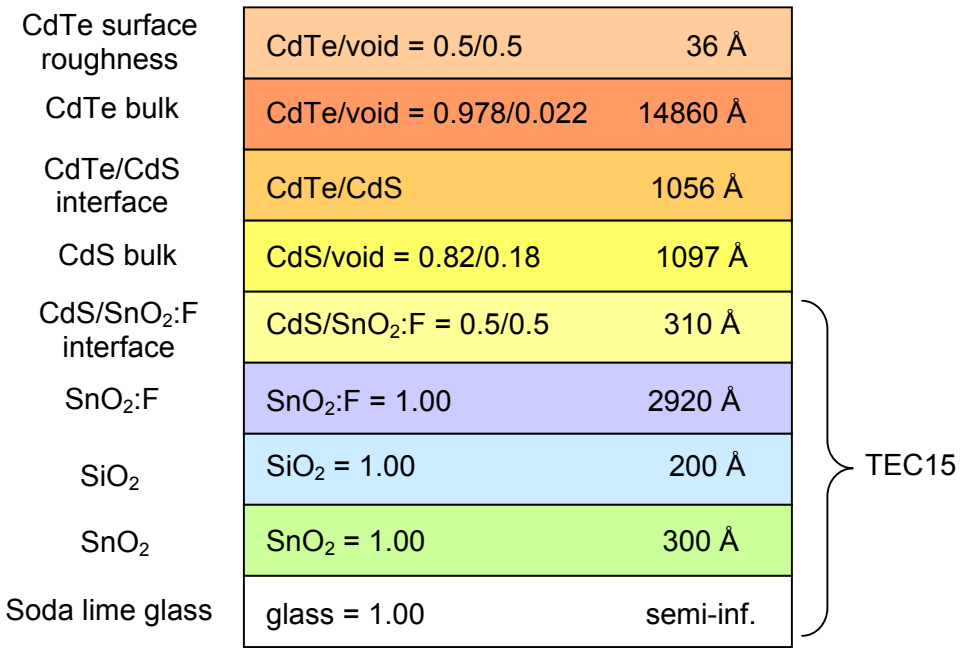

Fig. 4 Structural model for the CdTe solar cell that provides the best fit in Fig. 3.

The best fit model in Fig. 4 incorporates the glass substrate, including (i) a fixed optical structure for TEC-15, consisting of SnO_2 (300 Å); SiO_2 (200 Å); and SnO_2:F (2920 Å); (ii) an interfacial roughness layer between the TEC-15 and the CdS whose thickness is fixed to match the surface roughness thickness measured from the uncoated TEC-15 and whose composition is a fixed 0.5/0.5 effective medium mixture of the overlying and underlying materials; (iii) a CdS layer of variable thickness and void volume fraction; (iv) a single interface layer of variable thickness between the CdS and CdTe modeled as an effective medium of the two materials with variable composition; and (v) the bulk CdTe and its surface roughness layer, both of variable thickness. Because the starting TEC-15 transparent conductor layer exhibits an ~ 300 Å thick surface roughness layer, roughness is sure to propagate throughout the structure and thus occurs at each interface. As a result, any layers that are generated by the chemical interaction between the CdS and CdTe are modulated by roughness. Then a possible two-layer, three-interface chemical interaction region: [CdS/CdS:Te/CdTe:S/CdTe] would be converted by the modulated interfaces into an intractable five-layer, six interface region:
[CdS/(CdS+CdS:Te)/CdS:Te/(CdS:Te+CdTe:S)/CdTe:S/(CdTe:S+CdTe)/CdTe], where the mixed layers (A+B) represent a modulated interface converted to an interface roughness layer via an effective medium theory. Rather than trying to extract information using such a complex (although realistic) model, we use a single effective medium layer of CdS+CdTe of variable composition.

Among the interesting aspects of the results of Fig. 4 include:
(i) a ~1100 Å interface region of (CdS+CdTe) and
(ii) a significant void fraction in the CdS layer, (~0.18) measured relative to a dense CdS film deposited on smooth c-Si under similar conditions.
The effective composition of the mixed (CdS+CdTe) interface layer is ~0.7 CdS and ~0.3 CdTe; however, this mixture merely provides a dielectric function that approximates that of the interface region and should not be interpreted physically.

The significance of the conclusions (i) and (ii) can be tested by performing the same fits for all the spectra obtained as a function of CdTe bulk thickness during the etching steps. These fits should provide independent values for CdS/CdTe interface thickness and CdS void fraction since the raw data, i.e., pseudo-dielectric functions, vary rapidly versus CdTe bulk layer thickness due to changes in the interference pattern. In fact, these independent values should be constant since the etching does not affect the sub-surface material, and any variations provide a measure of the uncertainty in these values. For the conclusions above to be valid the uncertainties in interface thickness and void fraction must be smaller than the values themselves. Figures 5(a) and (b) show the results of these analyses, indicating that the CdS/CdTe interface layer thickness is ~1100±100 Å and the CdS void fraction is 0.20±0.09. Thus, the conclusions (i) and (ii) are supported by the independent analyses.

Future efforts on the depth profiling analysis will include:
(i) improvements in the technique, i.e., in both the model and fits, that narrow the confidence limits;
(ii) additional measurements from the glass side of the solar cell for higher sensitivity to the CdS and its interface to the CdTe.

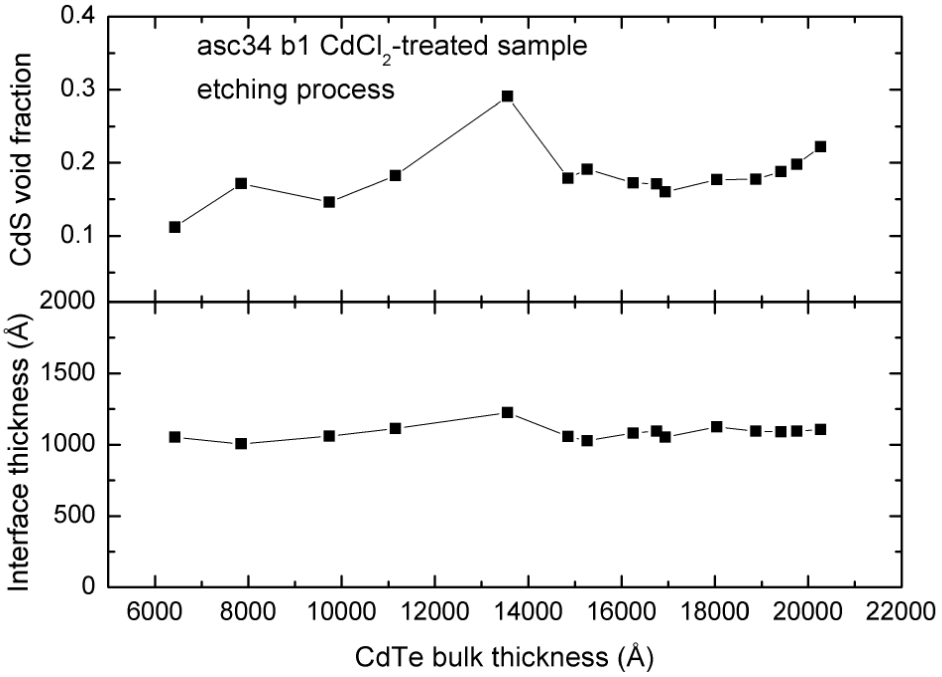

Fig. 5 Void volume fraction in the CdS layer and the thickness of the CdS+CdTe interface layer obtained in independent analyses of data at low energies during CdTe bulk layer etching. Because both layers are buried, these values should be constant and the variations provide the uncertainty.

Task 1.2.3. Nonuniformity loss in solar cell modules

In order to provide power generation suitable for practically important applications photovoltaic (PV) cells have to be integrated into large-area modules. If we represent such a module as a set of interconnected small area cells, then non-uniformity will result in variations between photovoltaic parameters of individual cells [1,2]. Even when there are no truly faulty elements, connecting cells with different PV parameters in a circuit will result in a mismatch power loss [3], since cells have to operate under current and voltage, different from the maximum power values. In a typical PV module thousands of cells with randomly distributed parameters form a complex network combining in-parallel and in-series connections. Estimate of non-uniformity related loss becomes then a nontrivial problem, further complicated by the effects of cell and interconnect resistances. A straightforward numerical power loss characterization, through comparison of an integrated module power output with the total power available from its constituent individual cells is implemented here based on the results obtained with PSpice software [4].

We address the following questions. How is the nonuniformity loss related to statistical and geometrical cell parameter distributions? What is the magnitude of the mismatch loss in a large area PV module and how it is scaled with a module size? What underlies the observed distribution of efficiencies in nominally identical production PV modules?

Equivalent circuit

In a typical integrated module, linear cells are connected in series [5] through metallized scribe lines (Fig.6a), which do not set tangible resistance between the cells. However, the typical cell length, of the order of tens of centimeters, can be large enough to make its different parts electrically disconnected. To account for the intra-cell nonuniformities one has to use an equivalent circuit where each linear cell is divided into a set of small sub-cells, connected in parallel. The linear size of such a sub-cell must be smaller than the characteristic length L, over which the electric potential can change noticeably. The latter can be estimated based on the well-known formula for the telegraph line, $L = a\sqrt{R_r / R_{TCO}}$ where $a \sim$ 1 cm is the cell width, $R_{TCO} \sim 10\ \Omega$ is the transparent conducting oxide (TCO) sheet resistance, and $R_r \sim 1\ \Omega$ is the metallized scribe resistance per unit length. This yields $L \sim 3$ cm, based on which we use in our equivalent circuit sub-cells of 1 by 1 cm connected as sketched in Fig.6b. Each sub-cell consists of a photodiode, characterized by its standard PV parameters, open-circuit voltage V_{oc} and short-circuit current J_{sc}, as well as series resistance R_s and shunt resistance R_{sh}.

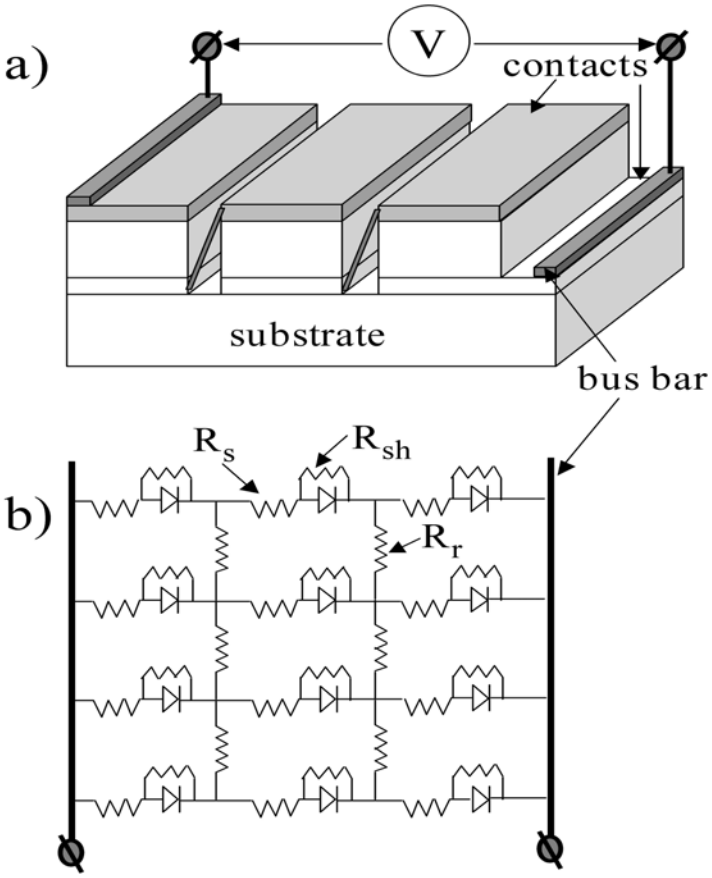

Fig. 6 a) Sketch of PV module with monolithic cell integration; b) equivalent circuit of integrated module: linear cells are connected in series through metallized scribes with resistance R_r along the scribe; each linear cell is represented as set of sub-cells connected in parallel; equivalent circuit for a sub-cell consists of photo-diode, series R_s and shunt R_{sh} resistances. A simplified case of 3 linear cells, each divided into 4 sub-cells, resulting in 3 by 4 sub-cells module is shown.

Modeling parameters

We used PSpice software to model circuits of 58 linear cells connected in series with each cell divided in 29 sub-cells corresponding, for example, to a realistic large area module of 2 by 1 ft with a sub-cell area of 1 cm^2. In addition, for size-dependent studies we used "square" modules of different sizes, ranging from 3 by 3 (total 9 sub-cells) to 35 by 35 (total 1225 sub-cells). Each sub-cell was assigned a set of PV parameters, one of which, either V_{oc} or J_{sc}, was fluctuating across the system. The fluctuating parameter distributions (example is shown in Fig. 7a) were randomly generated and characterized by their first three moments. In particular, for V_{oc} the moments are: average $<V_{oc}>$, standard deviation $SD(<V_{oc}>)=<(V_{oc}-<V_{oc}>)^2>^{1/2}$ or relative standard deviation $\delta(V_{oc})=<(V_{oc}-<V_{oc}>)^2>^{1/2}/<V_{oc}>$ and skewness $\gamma(V_{oc})=<(V_{oc}-<V_{oc}>)^3>^{1/3}$ / $SD(V_{oc})$.

The parameters used in this work were: $<V_{oc}>=755$ mV, $\delta V_{oc}=13\%$ ($SD(V_{oc})=100$ mV) and $\gamma(V_{oc})=-1.3$; $<J_{sc}>=21$ mA/cm^2, $\delta J_{sc}=13\%$, $\gamma(J_{sc})=-0.5$. Note, that negative γ is characteristic of asymmetric distributions with low-value tails. The rest of the parameters were $R_s=8.5\ \Omega$, $R_r=0.5\ \Omega$, $R_{sh}=10^5\ \Omega$.

For each distribution, the integral module current-voltage (J-V) characteristic was obtained and compared to that of the uniform module with sub-cell parameters equal to the averages over the corresponding fluctuating parameter distributions. We then calculated the resulting relative efficiency $\eta_{rel} = \eta_{non-uniform} / \eta_{uniform}$ as a figure of merit for the nonuniformity loss characterization.

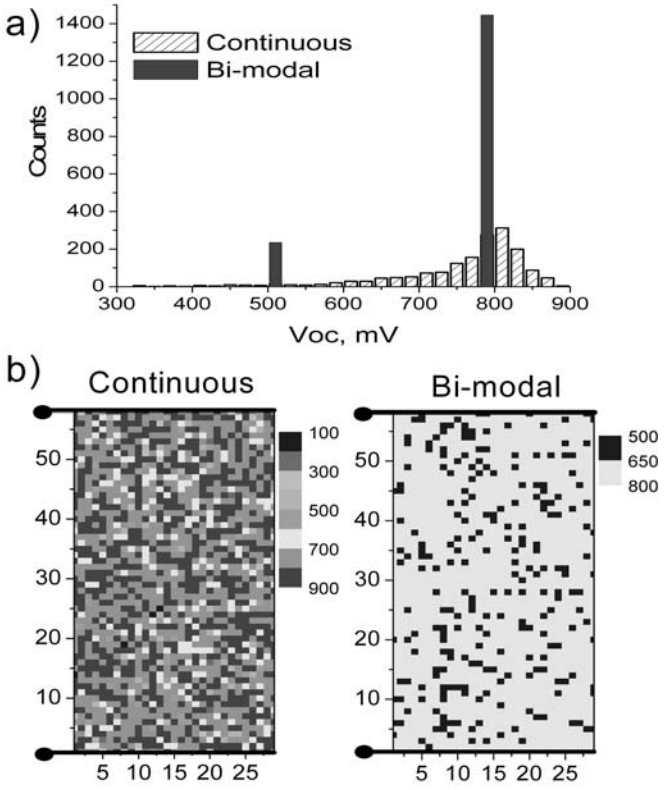

Fig. 7. a) Generated continuous and bi-modal V_{oc} distributions with the same first three moments: average value of 755 mV, standard deviation SD=100 (δV_{oc} =13%) and skewness γ=-1.3; b) V_{oc} maps of geometrical realization for corresponding statistical distributions. Relative efficiency for both is the same $\eta_{rel} = 0.92$.

Statistics vs. geometry

A set of N random sub-cells can be arranged into a module in a great number ($N!$) of geometrically different ways. A nontrivial result of this work is that the geometry plays almost no role when $N >> 1$, and a quite accurate estimate of the nonuniformity-related loss can be made based only on the information about the first three moments of the fluctuating parameter distribution.

More specifically, for a typical measured V_{oc} distribution in the form of the superposition of a Gaussian and a long low-value tail (continuous distribution in Fig. 7a), we have found that a module relative efficiency is practically independent of its geometrical implementation. As an example, the left side of Fig. 7b shows a geometrical implementation of a continuous distribution, each spot representing a V_{oc} value randomly assigned to the particular sub-cell in 58 by 29 module. We have simulated J-V curves for circuits with 20 different geometrical implementations of this statistical distribution, obtaining the same result for the relative efficiency with the accuracy better than 0.1%.

Moreover, a markedly different bi-modal distribution with the same first three moments (Fig. 7) also gives the same result for the relative efficiency. Given this invariance, we used the bi-modal distribution in simulations discussed below.

We have verified then that the latter surprising invariance holds when $N >> 1$, and the smaller N the stronger effect of geometry. For example, for the smallest module of 3 by 3 sub-cells (N=9) with only one element having V_{oc} or J_{sc} different from the rest, the resulting module efficiency depends strongly on that element's particular location. This leads to the highest standard deviation value for the relative efficiency (Fig. 8) of this module, calculated on a set of all possible configurations. For larger modules each point on the graph of Fig. 8 was obtained based on the efficiencies calculated for 20 modeled random geometrical realizations of statistically the same parameter distribution. As the module size increases, different geometrical realizations give closer values of efficiency and therefore lower value of SD. As shown in Fig. 8 for modules with N>100 the difference between geometrical realizations is almost negligible, ~1% or lower. From the practical standpoint, our finding shows that sub-modules of several tens of elements are quite representative statistically.

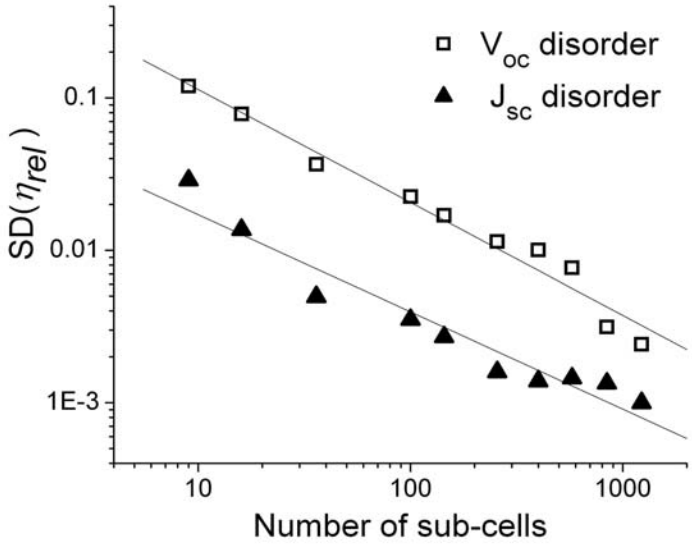

Fig. 8. Standard deviation (SD) of relative efficiency changes almost by 2 orders of magnitude from the smallest to the largest module (note a log-log scale). Solid lines show corresponding linear fits.

The dependence of the standard deviation *SD* on the module size, shown in Fig. 8, follows a scaling law $SD \propto N^{-\alpha}$ with $\alpha \approx 0.74$ for random V_{oc} and $\alpha \approx 0.64$ for random J_{sc} distributions. This points at nontrivial physics underlying our results (for example, one would expect $\alpha = 0.5$ for a superposition of mutually independent PV elements).

One consequence of the above established invariance is that it does not explain the observed distributions in efficiencies between production modules [6], which are typically rather broad, ~10% or more of their values. Indeed, if we assume that the modules are manufactured under the same conditions and therefore have the same statistical sub-cell parameter distributions, then our simulations predict the efficiency distributions narrower than 1% of their values, even when more than one parameter at a time is moderately (δ~13% in this work) fluctuating. Thus we have to take into account other factors, such as shunts and spots of low series resistance, located, for example, in the vicinity of metallized scribes or bus bars, not included in the above described modeling.

Mismatch loss

Traditionally the effect of nonuniformity was characterized in terms of mismatch loss [3], a difference between the sum of the maximum powers available from individual sub-cells and the maximum power output from the resulting circuit. Since calculated relative efficiency converges to a certain average value as the module size increases, so does the nonuniformity loss. We estimate the relative mismatch loss *m* (percentage of power lost due to mismatch) for modules of different sizes for the same statistical V_{oc} and J_{sc} distributions as described earlier (example for V_{oc} in Fig. 7a). The result in Fig. 9 shows indeed that for $N>>1$ a certain fraction of power, independent of *N,* is lost due to the mismatch. As expected from the diode equation, disorder in V_{oc} has a stronger effect.

The degree of disorder used in our simulations is rather moderate and representative of typical measured data [6]. For example, from Fig. 9 we find that only *m*=8% of power is lost for the case of V_{oc} disorder (δ=13%, γ=-1.5). However, this number goes up for more nonuniform modules; in particular, for δV_{oc}=30 % and the same $\langle V_{oc} \rangle$ and γ, we find *m* ~ 30%. An additional source of losses due to nonuniformity is associated with elements of low resistance as described below.

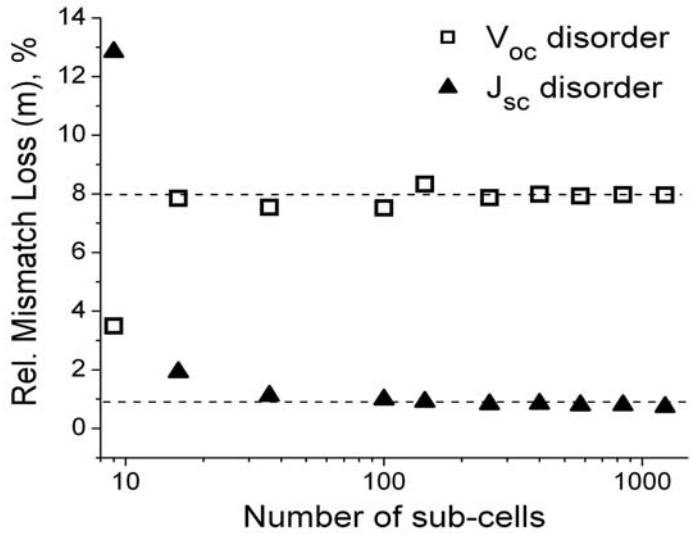

Fig. 9. Size dependence of the module mismatch loss for the cases of randomly distributed V_{oc} and J_{sc} with the relative deviations δ=13%.

Series and scribe resistances

Series and scribe resistances interfere with the nonuniformity effects. For a uniform module, it is well known that the series resistance loss lowers the efficiency. To the contrary, for a non-uniform module, lower value of R_s can enhance the efficiency loss [2,7], as shown in Fig.10.

Scribe resistance R_r has no effect on efficiency for the uniform module. However, low-resistive metallized scribes promote non-uniformity effects along the linear cells in the practically interesting range of R_s values, as illustrated in Fig. 10.

Shunting-like phenomena

So far we have discussed losses due to diode PV parameter distributions (V_{oc} and J_{sc}) with constant resistances across the system. In addition, our study shows that a strong detrimental effect on efficiency comes from occasional elements of low resistance. A dead shunt is one example of such an element. Another less trivial example is a sub-cell with a low series resistance in combination with low V_{oc} – we will call it a "hole", sometimes it is also referred to as a "non-ohmic shunt". To compare the effect of the two we calculated relative efficiency of a large (58 by 29) module, with a certain fraction of "damaged" elements – shunts (R_{sh}=0) or "holes" (R_s=0.01, V_{oc}=230 mV). The result in Fig. 11 shows similar losses in the range of practically reasonable fractions below 0.1.

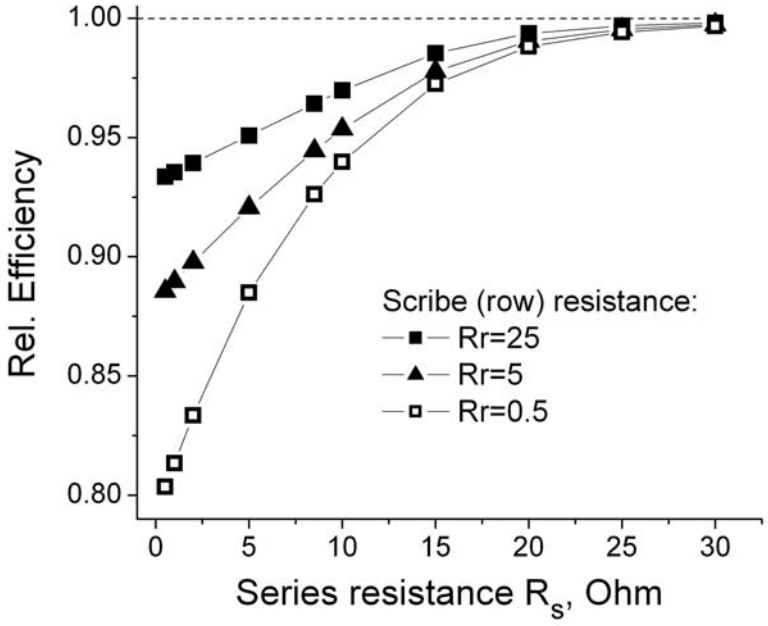

Fig. 10. Relative efficiency loss due to nonuniformity vs. series resistance R_s for different scribe resistances R_r. Modeled for disorder in V_{oc} with parameters as in Fig 2.

A comment is in order regarding the nature of "holes". The probability to find one in an integrated module is, in general, much higher than for a dead shunt, since spots of effectively low V_{oc} can occur often due to nonuniform penetrability of a front or back barrier [8]. When close to a metallized scribe or a bus bar, such element will have anomalously small lump series resistance R_s, becoming a "hole". Observations of such high current spots near the current collection channels seem to confirm this scenario even in crystalline Si modules [9].

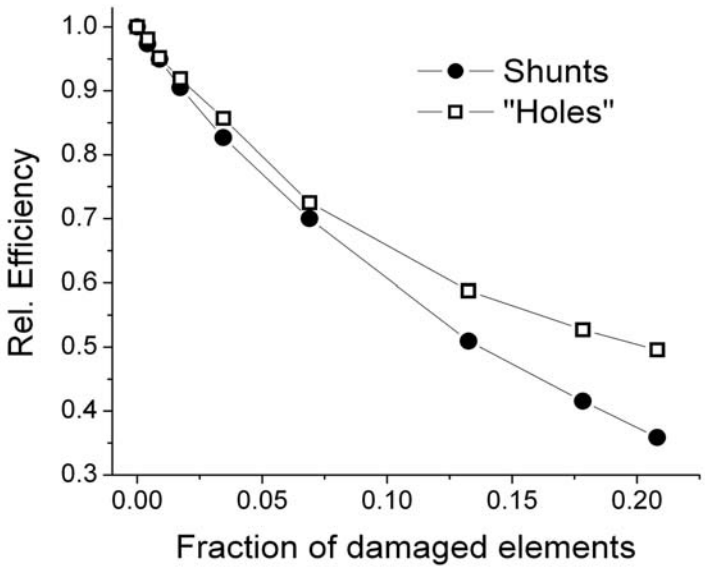

Fig. 11. Effect of the low-resistance elements - shunts (R_{sh}=0) and "holes" or "non-ohmic shunts" (R_s=0.01, V_{oc}=230 mV) - on the relative efficiency of a large module.

Conclusions

Nonuniformity effects in large-area PV modules exhibit several important features. i) Statistics of fluctuating parameter distribution plays the dominant role in resulting module efficiency; geometrical distribution of nonuniformities across the module has only a minor effect; ii) the module statistical characteristics exhibit non-trivial scaling dependencies vs. module size; iii) mismatch loss is close to a certain fraction of module power and is independent of the module size for a given statistical parameter distribution; iv) module series and scribe resistances interfere with nonuniformity effects offering a possibility to optimize combined nonuniformity and ohmic losses; v) shunting entities close to scribes and bus bars can be a significant efficiency loss factor.

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